SL3S4011_4021

UCODE I²C

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Product data sheet
COMPANY PUBLIC

1. General description

The UHF EPCglobal Generation 2 standard allows the commercialized provision of mass adoption of UHF RFID technology for passive smart tags and labels. Main fields of applications are supply chain management and logistics for worldwide use with special consideration of European, US and Chinese frequencies to ensure that operating distances of several meters can be realized.

The NXP Semiconductors UCODE product family is compliant to this EPC gen2 standard offering anti-collision and collision arbitration functionality. This allows a reader to simultaneously operate multiple labels/tags within its antenna field.

The UCODE based label/ tag requires no external power supply for contactless operation. Its contactless interface generates the power supply via the antenna circuit by propagative energy transmission from the interrogator (reader), while the system clock is generated by an on-chip oscillator. Data transmitted from the interrogator to the label/tag is demodulated by the interface, and it also modulates the interrogator's electromagnetic field for data transmission from the label/tag to the interrogator.

A label/tag can be then operated without the need for line of sight or battery, as long as it is connected to a dedicated antenna for the targeted frequency range. When the label/tag is within the interrogator's operating range, the high-speed wireless interface allows data transmission in both directions.

With the UCODE I^2C product, NXP Semiconductors introduces now the possibility to combine 2 independent UHF Interfaces (following EPC gen 2 standard) with an I^2C interface. Its large memory can be then read or write via both interfaces.

This I^2C functionality enables the standard EPC gen 2 functionalities to be linked to an electronic device microprocessor. By linking the rich functionalities of the EPC gen 2 standards to the Electronics world, the UCODE I^2C product opens a whole new range of application.

The I^2C interface needs to be supplied externally and supports standard and fast I^2C modes. Its large memory is based on a field proven non-volatile memory technology commonly used in high quality automotive applications

2. Features and benefits

2.1 UHF interface

- Dual UHF antenna port
- −18 dBm READ sensitivity
- −11 dBm WRITE sensitivity
- −23 dBm READ & WRITE sensitivity with the chip powered
- Compliant to EPCglobal Radio-Frequency Identity Protocols Class-1 Generation-2 UHF RFID Protocol for communications at 860 MHz to 960 MHz version 1.2.0
- Wide RF interface temperature range: −40 °C up to +85 °C
- Memory read protection
- Interrupt output
- RF - I^2C bridge function based on SRAM memory

2.2 I^2C interface

- Supports Standard (100 kHz) and Fast (400 kHz) mode (see Ref. 1)
- UCODE I^2C can be used as standard I^2C EEPROMs

2.3 Command set

- All mandatory EPC Gen2 v1.2.0 commands
- Optional commands: Access, Block Write (32 bit)
- Custom command: ChangeConfig

2.4 Memory

- 3328-bit user memory
- 160-bit EPC memory
- 96-bit tag identifier (TID) including 48-bit unique serial number
- 32-bit KILL password to permanently disable the tag
- 32-bit ACCESS password to allow a transition into the secured transmission state
- Data retention: 20 years at 55 °C
- Write endurance: 50 kcycles at 85 °C

2.5 Package

- SOT-902-3; MO-255B footprint
- Outline 1.6 × 1.6 mm
- Thickness ≤ 0.5 mm

3. Applications

- Firmware downloads
- Return management
- Counterfeit protection and authentication
- Production information
- Theft protection and deterrence
- Production automation
- Device customization/product configuration
- Offline Diagnostics

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SL3S4011FHK	XQFN8	Single differential RF Front End [1]- Plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm	SOT902-3
SL3S4021FHK	XQFN8	Dual differential RF Front End - Plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm	SOT902-3

[1] RFP1, RFN1

5. Block diagram

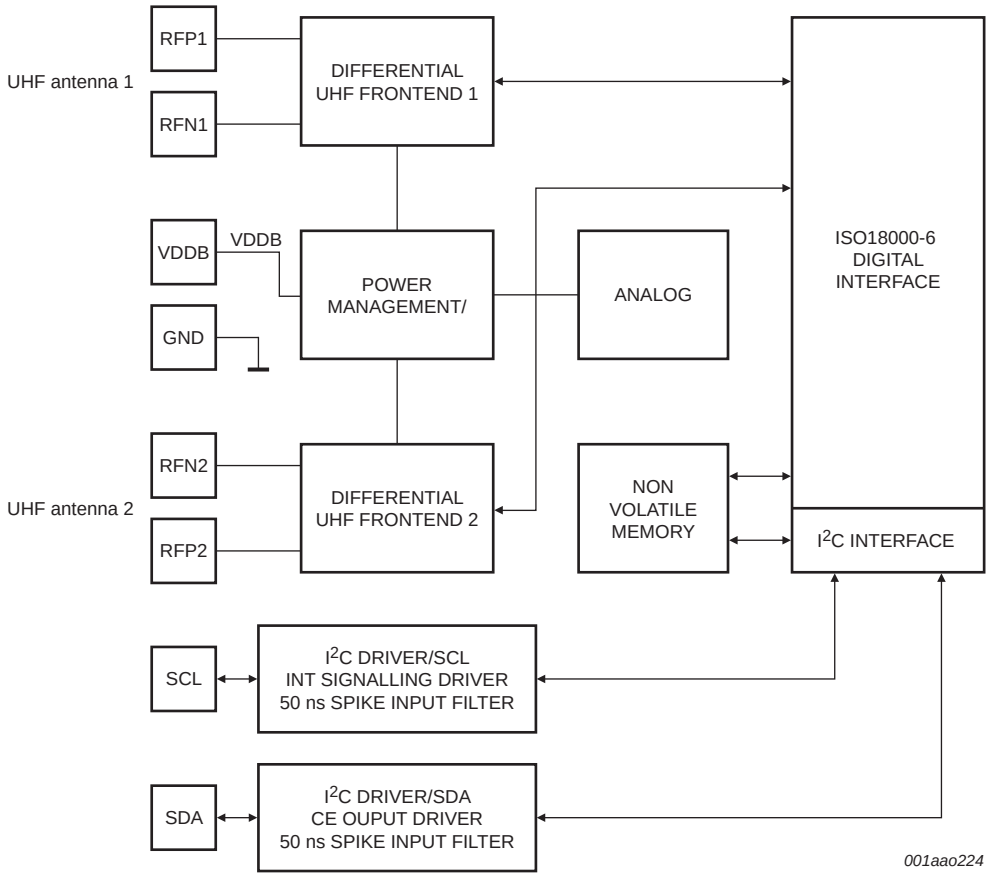
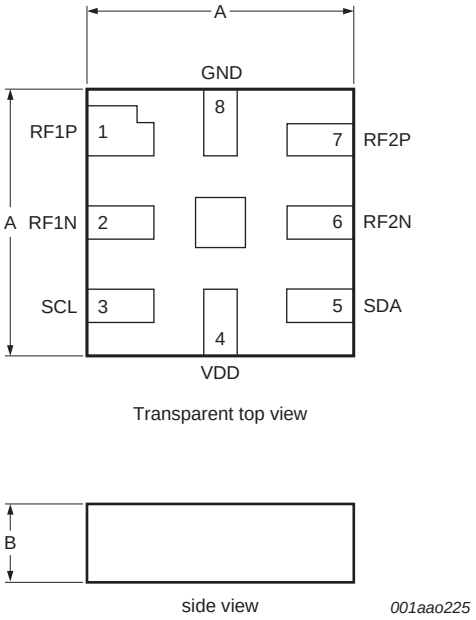


Fig 1. Block diagram

6. Pinning information

6.1 Pinning



(1) Dimension A: 1.6 mm

(2) Dimension B: 0.5 mm

Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Pin	Symbol	Description
1	RF1P	active antenna 1 connector
2	RF1N	antenna 1
3	SCL	I^2C clock / _INT
4	VDD	supply
5	SDA	I^2C data
6	RF2N	antenna 2
7	RF2P	active antenna 2 connector
8	GND	ground

7. Mechanical specification

7.1 SOT902 specification

Table 3. Mechanical properties XQFN8

Package name	Outline code	Package size	Reel format
SOT902	SOT902-3	size:1.6 mm × 1.6 mm	4000 pcs
		thickness: 0.5 mm	7” diameter
			Carrier tape width 8 mm
			Carrier pocket pitch 4 mm

8. Functional description

8.1 Air interface standards

The UCODE I²C fully supports all mandatory parts of the "Specification for RFID Air Interface EPCglobal, EPC Radio-Frequency Identity Protocols, Class-1 Generation-2 UHF RFID, Protocol for Communications at 860 MHz to 960 MHz, Version 1.2.0".

8.2 Power transfer

The interrogator provides an RF field that powers the tag, equipped with a UCODE I²C. The antenna transforms the impedance of free space to the chip input impedance in order to get the maximum possible power for the UCODE I²C on the tag.

The RF field, which is oscillating on the operating frequency provided by the interrogator, is rectified to provide a smoothed DC voltage to the analog and digital modules of the IC.

For I²C operation the UCODE I²C has to be supplied externally via the VDD pin.

8.3 Data transfer air interface

8.3.1 Interrogator to tag Link

An interrogator transmits information to the UCODE I²C by modulating a UHF RF signal. The UCODE I²C receives both information and operating energy from this RF signal. Tags are passive, meaning that they receive all of their operating energy from the interrogator's RF waveform.

An interrogator is using a fixed modulation and data rate for the duration of at least one inventory round. The interrogator communicates to the UCODE I²C by modulating an RF carrier using DSB-ASK with PIE encoding.

8.3.2 Tag to reader Link

An interrogator receives information from a UCODE I²C by transmitting an unmodulated RF carrier and listening for a backscattered reply. The UCODE I²C backscatters by switching the reflection coefficient of its antenna between two states in accordance with the data being sent.

The UCODE I²C communicates information by backscatter-modulating the amplitude and/or phase of the RF carrier. Interrogators shall be capable of demodulating either demodulation type.

The encoding format, selected in response to interrogator commands, is either FM0 baseband or Miller-modulated subaltern.

8.4 Data transfer to I²C interface

The UCODE I²C memory can be read/written similar to a standard I²C serial EEPROM device. The address space is arranged in a linear manner. When performing a sequential read the address pointer is increased linearly from start of the EPC memory to the end of the user memory.

At the end address of each bank the address pointer jumps automatically to the first address in the subsequent bank. In I²C write modes only even address values are accepted, due to the word wise organization of the EEPROM.

Regarding arbitration between RF and I²C, see Section 11 “RF interface/I²C interface arbitration”).

Write operation:

- Write word
- Write block (2 words)

Read operation:

- current address read
- random address read
- sequential current read
- random sequential read

8.5 Supported commands

The UCODE I²C supports all mandatory EPCglobal V1.2.0 commands.

In addition the UCODE I²C supports the following optional commands.

- Access
- BlockWrite (32 bit)

The UCODE I²C features the following custom commands described in more detail later:

- ChangeConfig

8.6 UCODE I²C memory

The UCODE I²C memory is implemented according to EPCglobal Gen2 and organized in four sections all accessible via both RF and I²C operation except the reserved memory section which only accessible via RF:

Table 4. UCODE I²C memory sections

Name	Size	Bank
Reserved memory (32-bit ACCESS and 32-bit KILL password)	64 bit	00b
EPC (excluding 16 bit CRC-16 and 16-bit PC)	160 bit	01b
Download register	16 bit	01b
UCODE I²C Configuration Word	16 bit	01b
TID (including unique 48 bit serial number)	96 bit	10b
User Memory	3328 bit	11b

The logical addresses of all memory banks begin at zero (00h).

In addition to the 4 memory banks one configuration word to handle the UCODE I²C specific features is available at EPC bank 01b address 200h. The configuration word is described in detail in section “UCODE I²C special features”.

8.6.1 UCODE I²C overall memory map

Table 5. Memory map

Bank address	Memory address		Type	Content	Initial value	Remark
	RF	I²C				
Bank 00	00h to 1Fh	not accessible via i²C	reserved	kill password	all 00h	unlocked memory
	20h to 3Fh	not accessible via i²C	reserved	access password	all 00h	unlocked memory
Bank 01 EPC	00h to 0Fh	2000h	EPC	CRC-16: refer to Ref. 5		memory mapped calculated CRC
	10h to 1Fh	2002h	EPC	PC	3000h	unlocked memory
	20h to 2Fh	2004h	EPC	EPC bit [0 to 15]	[1]	unlocked memory
	...		EPC	...		unlocked memory
	20h to BFh	2016h	EPC	EPC bit [144 to 159]		unlocked memory
	1F0h to 1FFh	203Eh	EPC	download register		for the bridge function
	200h to 20Fh	2040h	EPC	Configuration word, see Section 9.2		
Bank 10 TID	00h to 0Fh	4000h	TID	TID header	n.a.	locked memory
	10h to 1Fh	4002h	TID	TID header	n.a.	locked memory
	20h to 2Fh	4004h	TID	XTID_header	0000h	locked memory
	30h to 3Fh	4006h	TID	TID serial number	[2]	locked memory
	40h to 4Fh	4008h	TID	TID serial number	n.a.	locked memory
	50h to 5Fh	400Ah	TID	TID serial number	n.a.	locked memory
Bank 11 User memory	000h to 00Fh	6000h	UM	user memory bit [0 to 15]	all 00h	unlocked memory
	010h to 01Fh	6002h	UM	user memory bit [16 to 31]	all 00h	unlocked memory
	...		UM		all 00h	unlocked memory
	CF0h to CFFh	619Eh	UM	user memory bit [3311 to 3327]	all 00h	unlocked memory

[1] SL3S4011 EPC: E200 680D 0000 0000 0000 0000 0000 0000 0000 0000
SL3S4021 EPC: E200 688D 0000 0000 0000 0000 0000 0000 0000 0000

[2] see TID paragraph

8.6.2 UCODE I²C TID memory details

Table 6. UCODE I²C TID description

Type	First 32 bit of TID memory	Class ID	Mask designer ID	Model number		
				Config Word indicator	Sub version number	Version (Silicon) number
UCODE SL3S4011	E200680D	E2h	006h	1	0000b	0001101
UCODE SL3S4021	E200688D	E2h	006h	1	0001b	0001101

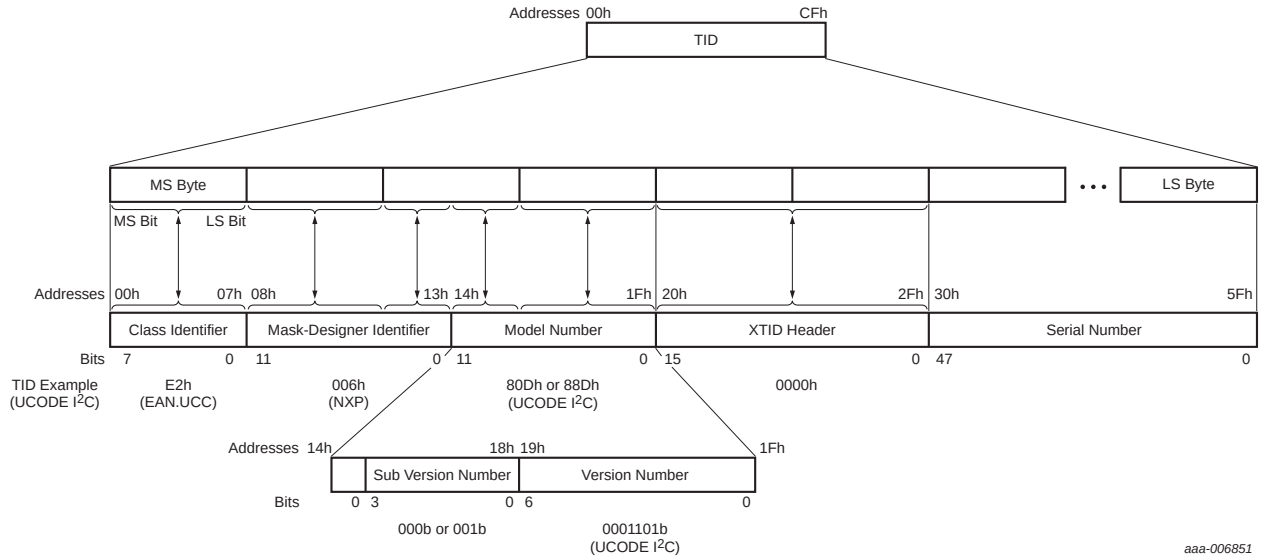


Fig 3. UCODE I²C TID memory structure

9. Supported features

The UCODE I²C is equipped with a number of additional features and a custom command. Nevertheless, the chip is designed in a way that standard EPCglobal READ / WRITE / ACCESS commands can be used to operate the features.

The memory map in the previous section describes the Configuration Word used to control the additional features located after address 200h of the EPC memory, hence UCODE I²C features are controlled by bits located in the EPC number space. For this reason the standard READ / WRITE commands of a UHF EPCglobal compliant reader can be used to select the flags or activate/deactivate features if the memory bank is not locked. In case of locked memory banks the ChangeConfig custom command has to be used.

The bits (flags) of the ConfigurationWord are selectable using the standard EPC SELECT command.

9.1 UCODE I²C special feature

- **Externally Supplied flag**
  The flag will indicate the availability of an external supply.
- **RF active flag**
  The flag will indicate on which RF port power is available and signal transmission ongoing.
- **RF Interface on/off switching**
  For privacy reasons the two RF ports as well as the I²C interface can be switched on/off by toggling the related bits of the ConfigurationWord. The ConfigurationWord is accessible via RF and I²C interface. Although it is possible to kill the RF interface via the KILL feature of EPC gen2, a minimum of one port shall be active at all times. In the case of the dual port version, either one or both RF can be active. In the case of the single front end version, the RF port can not be deactivated.
- **I²C Interface on/off switching**
  For privacy reasons the I²C port can be disabled by toggling the related bit of the Config-Word but only via RF.
- **RF - I²C Bridge feature**
  The UCODE I²C can be used as an RF- I²C bridge to directly forward data from the RF interface to the I²C interface and vice versa. The UCODE I²C is equipped with a download/upload register of 16-bit data buffer located in the EPC bank. The data received via RF can be read via I²C like regular memory content. In case the buffer is empty reading the register returns NAK. This feature can be combined with the Download Indicator.
  - **Upload Indicator flag** (I²C to UHF) - address 203h in the configuration word
    The flag will indicate if data in the download/upload register is available. Will be automatically cleared when the download/upload register is read out via UHF.
  - **Download Indicator flag** (UHF to I²C) - address 200h in the configuration word
    The flag will indicate if data in the download/upload register is available. Will be automatically cleared when the download/upload register is read out via I²C.

- **Interrupt signaling/Download Indicator**
  The UCODE I²C features two methods of signaling:

  1. Signaling via ConfigWord "Download/Upload Indicator" (200h or 203h):
  - The Download/Upload Indicator will go high as soon new data from the RF reader or from the I²C interface is written to the buffer register. This flag can be polled via I²C READ or using the SELECT command. Reading an empty buffer register will return NAK.
  - The Download/Upload Indicator will automatically return to low as soon as the data is read.

  2. Interrupt Signaling via the I²C-SCL line:
  - If the SCL INT enabler of the ConfigWord is set (20Bh) the SCL line will be pulled low for at least 210 µs in case new data was written by the reader or at least 85 µs in case new data has been read by the reader (see Figure 4 “SCL interrupt signalling” and Table 7 “Interrupt signaling via the I2C-SCL line timing”).

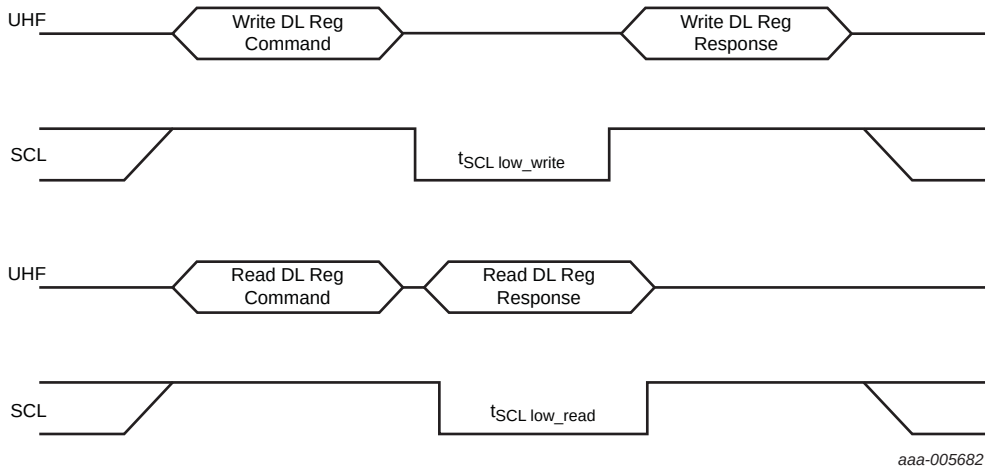


Fig 4. SCL interrupt signalling

Table 7. Interrupt signaling via the I2C-SCL line timing

Symbol	Min	Typ	Max	Unit
$t_{SCL\ low\_write}$	210	266	320	µs
$t_{SCL\ low\_read}$[1]	85	102[2]	7800	µs

[1] This timing parameter is dependent on the chosen return link frequency.

[2] At 640 kHz return link frequency.

Remark: The features can even be operated (enabled/disabled) with '0' as ACCESS password. It is recommended to set an ACCESS password to avoid unauthorized manipulation of the features via the RF interface.

9.2 UCODE I²C special features control mechanism

Special features of the UCODE I²C are managed using a Configuration Word (ConfigWord) located at the end of the EPC memory bank (address 200h via RF or 2040h via I²C) - see Table 8 and Table 9.

The bits of the ConfigWord are selectable (using the standard EPC SELECT command) and can be read, via RF, using standard EPC READ command and via I²C. They can be modified using the ChangeConfig custom command or standard READ/WRITE commands or via the I²C interface (if allowed).

Table 8. Configuration Word accessible located at address 200h via UHF of the EPC bank and I²C address 2040h (1 RF front end version SL3S4011)

Feature	Bit type	via RF		via I²C	
		Address	Access	Address	Access
Download indicator	indicator[1]	200h	read	2040h	read
Externally supplied flag	indicator	201h	read		read
RF active flag	indicator	202h	read		read
Upload indicator	Indicator	203h	read		read
I²C address bit 3[3]	permanent[2]	204h	r/w		read only
I²C address bit 2[3]	permanent	205h	r/w		read only
I²C address bit 1[3]	permanent	206h	r/w		read only
I²C port on/off	permanent	207h	r/w		read only
UHF antenna port1 on	locked	208h	read only		read only
rfu		209h			
rfu		20Ah			
SCL INT enable	permanent	20Bh	r/w		read only
bit for read protect user memory	permanent	20Ch	r/w		r/w
bit for read protect EPC	permanent	20Dh	r/w		r/w
bit for read protect TID SNR (48 bits)	permanent	20Eh	r/w		r/w
PSF alarm flag	permanent	20Fh	r/w		read only

[1] Indicator bits are reset at power-up but cannot be changed by command

[2] Permanent bits are permanently stored bits in the memory

[3] Defaults values for bit3/bit2/bit1 are 0/0/1 (see Table 14)

Table 9. Configuration Word accessible located at address 200h via UHF of the EPC bank and I²C address 2040h (2 RF front end version SL3S4021)

Feature	Bit type	via RF		via I²C	
		Address	Access	Address	Access
Download indicator	indicator[1]	200h	read	2040h	read
Externally supplied flag	indicator	201h	read		read
RF active flag	indicator	202h	read		read
Upload indicator	indicator	203h	read		read
I²C address bit 3[3]	permanent[2]	204h	r/w		read only
I²C address bit 2[3]	permanent	205h	r/w		read only
I²C address bit 1[3]	permanent	206h	r/w		read only
I²C port on/off	permanent	207h	r/w		read only
UHF antenna port1 on/off	permanent	208h	r/w		r/w
UHF antenna port2 on/off	permanent	209h	r/w		r/w
rfu		20Ah			

Table 9. Configuration Word accessible located at address 200h via UHF of the EPC bank and I²C address 2040h (2 RF front end version SL3S4021)

Feature	Bit type	via RF		via I²C	
		Address	Access	Address	Access
SCL INT enable	permanent	20Bh	r/w		read only
bit for read protect user memory	permanent	20Ch	r/w		r/w
bit for read protect EPC	permanent	20Dh	r/w		r/w
bit for read protect TID SNR (48 bits)	permanent	20Eh	r/w		r/w
PSF alarm flag	permanent	20Fh	r/w		read only

[1] Indicator bits are reset at power-up but cannot be changed by command

[2] Permanent bits are permanently stored bits in the memory

[3] Defaults values for bit3/bit2/bit1 are 0/0/1 (see Table 14)

9.3 Change Config Command

The UCODE I²C ChangeConfig custom command allows handling the special features described in the previous paragraph. As long the EPC bank is not write locked standard EPC READ/WRITE commands can be used to modify the flags.

Table 10. ChangeConfig custom command

	Command	RFU	Data	RN	CRC-16
No. of bits	16	8	16	16	16
Description	11100000 00000111	00000000	Toggle bits XOR RN16	handle	-

The bits to be toggled in the configuration register need to be set to '1'.

E.g. sending 0000 0000 0000 0000 1001 XOR RN16 will activate the EPC Read Protect and PSF bit. Sending the very same command a second time will disable the features.

The reply of the ChangeConfig will return the current register setting.

Table 11. ChangeConfig custom response table

Starting state	Condition	Response	Next state
ready	all	-	ready
arbitrate, reply, acknowledged	all	-	arbitrate
open	valid handle, Status word needs to change	Backscatter unchanged StatusWord immediately	open
	valid handle, Status word does not need to change	Backscatter StatusWord immediately	open
secured	valid handle, Status word needs to change	Backscatter modified StatusWord, when done	secured
	valid handle, Status word does not need to change	Backscatter StatusWord immediately	secured
	invalid handle	-	secured
killed	all	-	killed

The features can only be activated/deactivated in the open or secured state and with a non-zero ACCESS password. If the EPC memory bank is locked for writing, the ChangeConfig command is needed to modify the ConfigurationWord.

9.4 UCODE I²C memory bank locking mechanism

9.4.1 Possibilities

Table 12. Memory banks locking possibilities for UCODE I²C via RF and I²C

Memory bank		I²C interface		RF interface	
		Lock (entire bank)	PermaLock (entire bank)	Lock (entire bank) via Access Password	PermaLock (entire bank) via Access Password
01	EPC	yes	yes	yes	yes
11	User Memory	yes	yes	yes	yes

9.4.2 Via RF

The UCODE I²C memory banks can be locked following EPC Gen2 mandatory command via RF (see table Table 13).

Table 13. Lock payload and usage

	Kill pwd		Access pwd		EPC memory		TID memory		User memory	
	19	18	17	16	15	14	13	12	11	10
Mask	skip/write	skip/write	skip/write	skip/write	skip/write	skip/write	skip/write	skip/write	skip/write	skip/write
	9	8	7	6	5	4	3	2	1	0
Action	pwd read/write	permalock	pwd read/write	permalock	pwd write	permalock	pwd write	permalock	pwd write	permalock

9.4.3 Via I2C

The EPC Gen2 locking bits for the memory banks are also accessible via the I²C interface for read and write operation and are located at the I²C address 803Ch. But it is not possible to read and write the access and kill password.

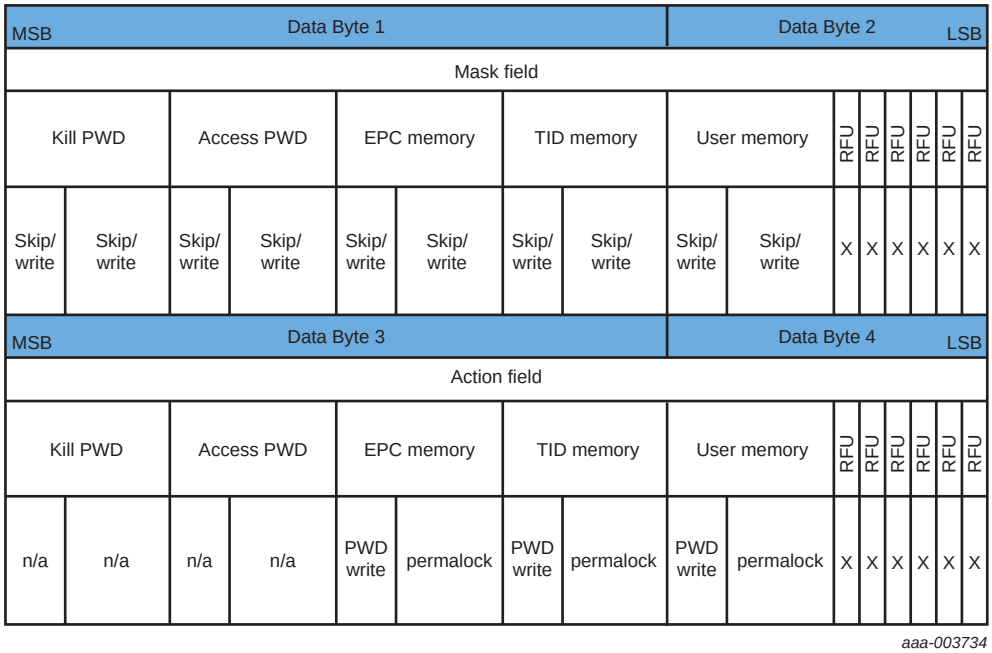


Fig 5. I²C memory bank lock write and read access

10. I²C commands

10.1 UCODE I²C operation

For details on I²C interface refer to Ref. 1.

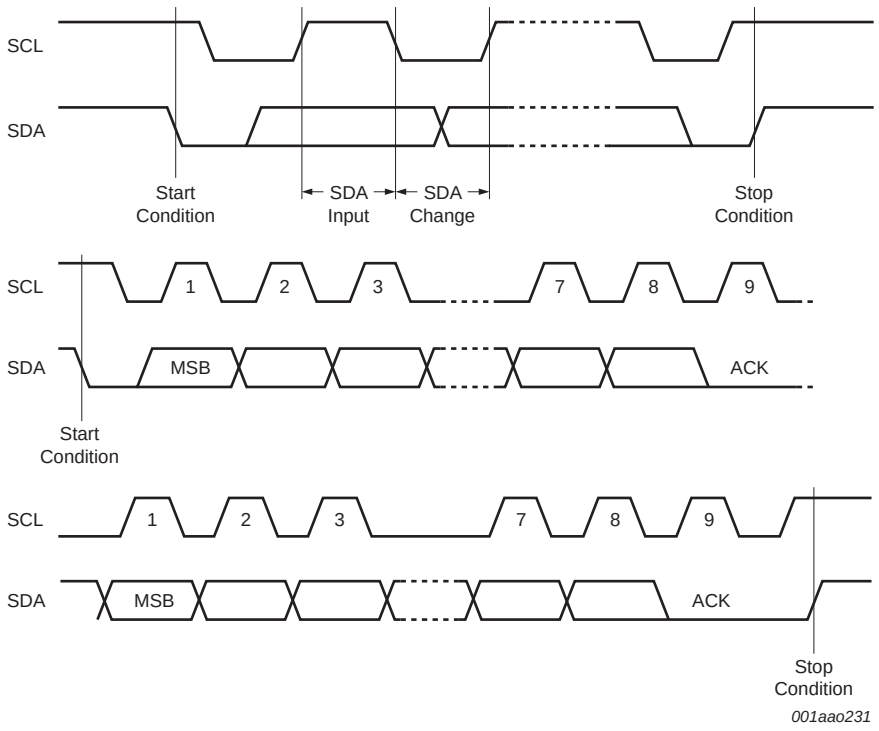


Fig 6. I²C bus protocol

The UCODE I²C supports the I²C protocol. This is summarized in Figure 7. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always a slave in all communications.

10.2 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer command. The UCODE I²C continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

10.3 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the UCODE I²C and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the UCODE I²C into the Standby mode. A Stop condition at the end of a Write command triggers the internal Write cycle.

10.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

10.5 Data input

During data input, the UCODE I²C samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change only when Serial Clock (SCL) is driven low.

10.6 Addressing

To start communication between a bus master and the UCODE I²C slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code. The 7-bit device select code consists of a 4-bit device identifier (value Ah) which is initialized in wafer test and cannot be changed in the user mode. Three additional bits in the configuration word are reserved to alter the device address via RF interface after initialization. This allows up to eight UCODE I²C devices to be connected to a bus master at the same time.

The 8th bit is the Read/Write bit (RW). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device select code, the UCODE I²C gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the UCODE I²C does not match the device select code, it deselects itself from the bus.

Table 14. Device select code

	Device type identifier				Device address in configuration word 204h to 206h			R/W
Device select code	b7	b6	b5	b4	b3	b2	b1	b0
Value	1	0	1	0	0 [1]	0 [1]	1 [1]	1/0

[1] Initial values - can be changed - See also Table 8 and Table 9.

Table 15. I²C addressing

Most significant byte	b15	b14	b13	b12	b11	b10	b9	b8
EPC address	EPC/Lock	EPC memory bank		EPC memory word address				
Least significant byte	b7	b6	b5	b4	b3	b2	b1	b0
EPC address	EPC memory word address							MSB/ LSB

10.7 Write Operation

The byte address must be an even value due to the word wise organization of the EEPROM.

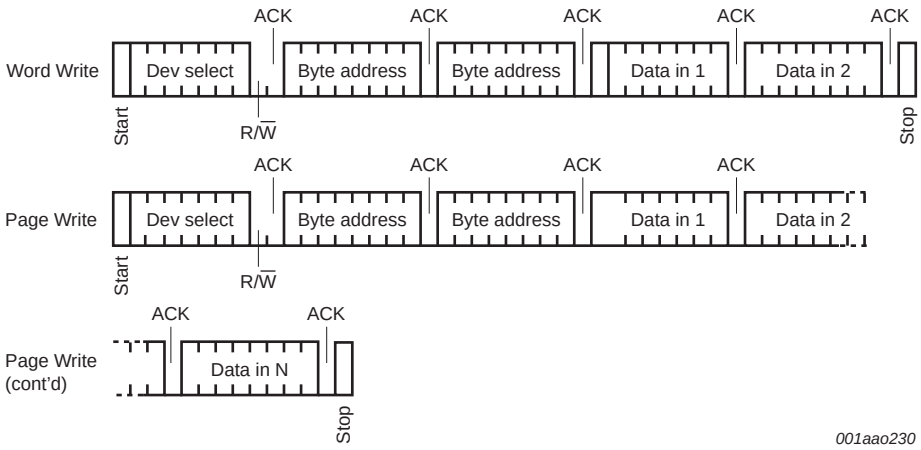


Fig 7. I²C write operation

Following a Start condition the bus master sends a device select code with the Read/Write bit (RW) reset to 0. The UCODE I²C acknowledges this, as shown in Figure 7 and waits for two address bytes. The UCODE I²C responds to each address byte with an acknowledge bit, and then waits for the data Byte.

Each data byte in the memory has a 16-bit (two byte wide) address. The Most Significant Byte (Table 15) is sent first, followed by the Least Significant Byte (Table 15). Bits b15 to b0 form the address of the byte in memory.

When the bus master generates a Stop condition immediately after the ACK bit (in the "10th bit" time slot), either at the end of a Word Write or a Page Write, the internal Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) is disabled internally, and the UCODE I²C does not respond to any requests.

10.7.1 Word Write

After the device select code and the address word, the bus master sends one word data. If the addressed location is Write-protected, the UCODE I²C replies with NACK, and the location is not modified. If, instead, the addressed location is not Write-protected, the UCODE I²C replies with ACK. The bus master terminates the transfer by generating a Stop condition, as shown in Figure 7.

10.7.2 Page Write

The Page Write mode allows 2 words to be written in a single Write cycle, provided that they are all located in the same 'row' in the memory: that is, the most significant memory address bits (b12-b2) are the same and b1= 0 and b0 = 0. If more than two words are sent than each additional byte will cause a NACK on SDA.

The bus master sends from 1 to 2 words of data, each of which is acknowledged by the UCODE I²C. The transfer is terminated by the bus master generating a Stop condition.

10.8 Read operation

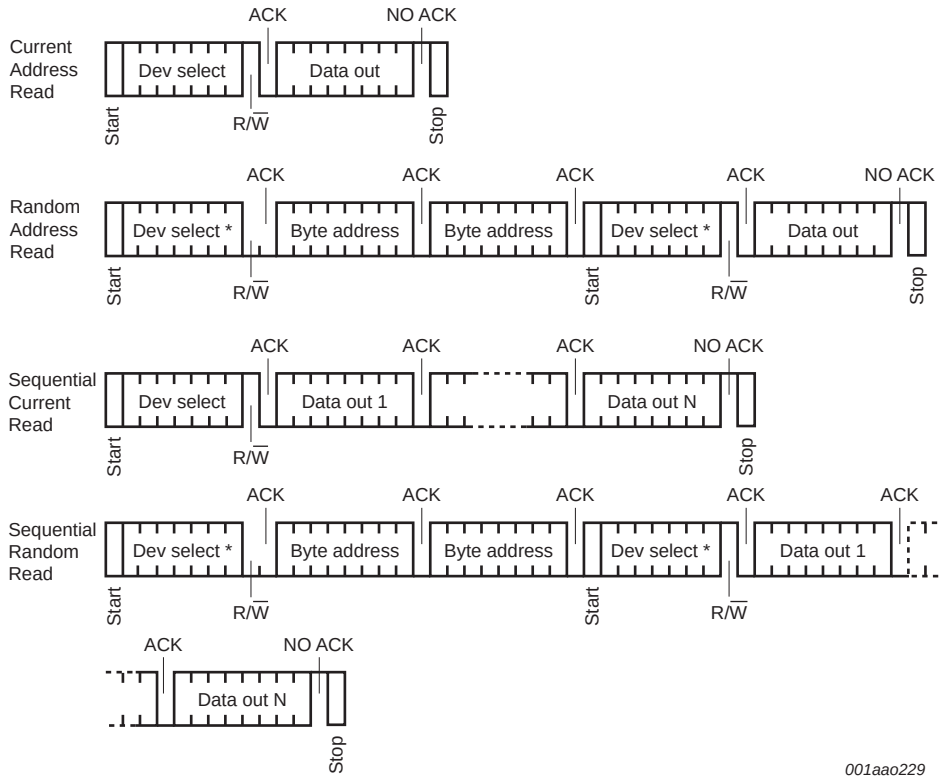


Fig 8. I²C read operation

After the successful completion of a read operation, the UCODE I²C's internal address counter is incremented by one, to point to the next byte address.

10.8.1 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in Figure 8) but without sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the Read/Write bit (RW) set to 1. The UCODE I^2C acknowledges this, and outputs the contents of the addressed byte. The bus master must not acknowledge the byte, and terminates the transfer with a Stop condition.

10.8.2 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a UCODE I^2C select code with the Read/Write bit (RW) set to 1. The UCODE I^2C acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in Figure 8, without acknowledging the Byte.

10.8.3 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master does acknowledge the data byte output, and sends additional clock pulses so that the UCODE I^2C continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must not acknowledge the last byte, and must generate a Stop condition, as shown in Figure 8.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output.

10.8.4 Acknowledge in Read mode

For all Read commands, the UCODE I^2C waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) low during this time, the UCODE I^2C terminates the data transfer and switches to its Standby mode.

10.8.5 EPC memory bank handling

After the last memory address within one EPC memory bank, the address counter 'rolls-over' to the next EPC memory bank, and the UCODE I^2C continues to output data from memory address 00h in the successive EPC memory bank.

Example: EPC Bank 01 → EPC Bank 10 → EPC Bank 11 → EPC Bank 01

11. RF interface/I²C interface arbitration

The UCODE I²C needs to arbitrate the EEPROM access between the RF and the I²C interface.

The arbitration is implemented as following:

- First come, first serve strategy - the interface which provides data by having a first valid preamble on RF envelope (begin of a command) or a start condition and a valid I²C device address on the I²C interface will be favored.
- I²C access to the chip memory is possible regardless if it is in the EPC Gen2 secured state or not
- During an I²C command, starting with an I²C start followed by valid I²C device address and ending with an I²C stop condition, any RF command is ignored.
- During any EPC Gen2 command any I²C command is ignored

12. Limiting values

Table 16. Limiting values[1][2] [3][4]

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
Die					
V_{max}	maximum voltage	on pin VDD, SDA, SCL, GND	–0.3	3.6	V
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{ESD}	electrostatic discharge voltage	Human body model; SNW-FQ-302A	-	±2	kV
		Charged device model	-	±500	V

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Operating Conditions and Electrical Characteristics section of this specification is not implied.

[2] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.

[3] For ESD measurement, the die chip has been mounted into a CDIP8 package.

[4] For ESD measurement, the die chip has been mounted into a CDIP8 package.

13. Characteristics

Table 17. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
EEPROM characteristics						
t_{ret}	retention time	$T_{amb} \leq 55$ °C	20	-	-	year
$N_{endu(W)}$	write endurance	$T_{amb} \leq 85$ °C	50000	-	-	cycle
Interface characteristics						
P_{tot}	total power dissipation		-	-	30	mW
f_{oper}	operating frequency		840	-	960	MHz
P_{min}	minimum operating power supply	Read mode	-	–18	-	dBm
		Write mode	-	–11	-	dBm
		Read and Write mode with V_{DD} input	-	–23	-	dBm
V_{DD}	supply voltage	I^2C, on V_{DD} input	1.8	-	3.6	V
V_{DD}	supply voltage rise time requirements		100	-	-	µs
I_{DD}	supply current	from VDD in I^2C read mode	-	10	-	µA
		from VDD in I^2C write mode	-	40	-	µA
Z	impedance (package)	915 MHz	-	12,7-j 199	-	Ω
-	modulated jammer suppression ≥ 1.0 MHz		-	–4	-	dB
-	unmodulated jammer suppression ≥ 1.0 MHz		-	–4	-	dB
V_{IL}	LOW-level input voltage[1]		-0.5	-	0.3 V_{DD}	V
V_{IH}	HIGH-level input voltage[1]		0.7 V_{DD}	-	-[2]	V
V_{hys}	hysteresis of Schmitt trigger inputs[4]		0.05 V_{DD}	-	-	V
V_{OL1}	LOW-level output voltage 1	(open-drain or open-collector) at 3 mA sink current[3]; $V_{DD} > 2$ V	0	-	0.4	V
V_{OL2}	LOW-level output voltage 2[4]	(open-drain or open-collector) at 2 mA sink current[3]; $V_{DD} \leq 2$ V	0	-	0.2V_{DD}	V

[1] Some legacy Standard-mode devices had fixed input levels of V_{IL} = 1.5 V and V_{IH} = 3.0 V. Refer to component data sheets.

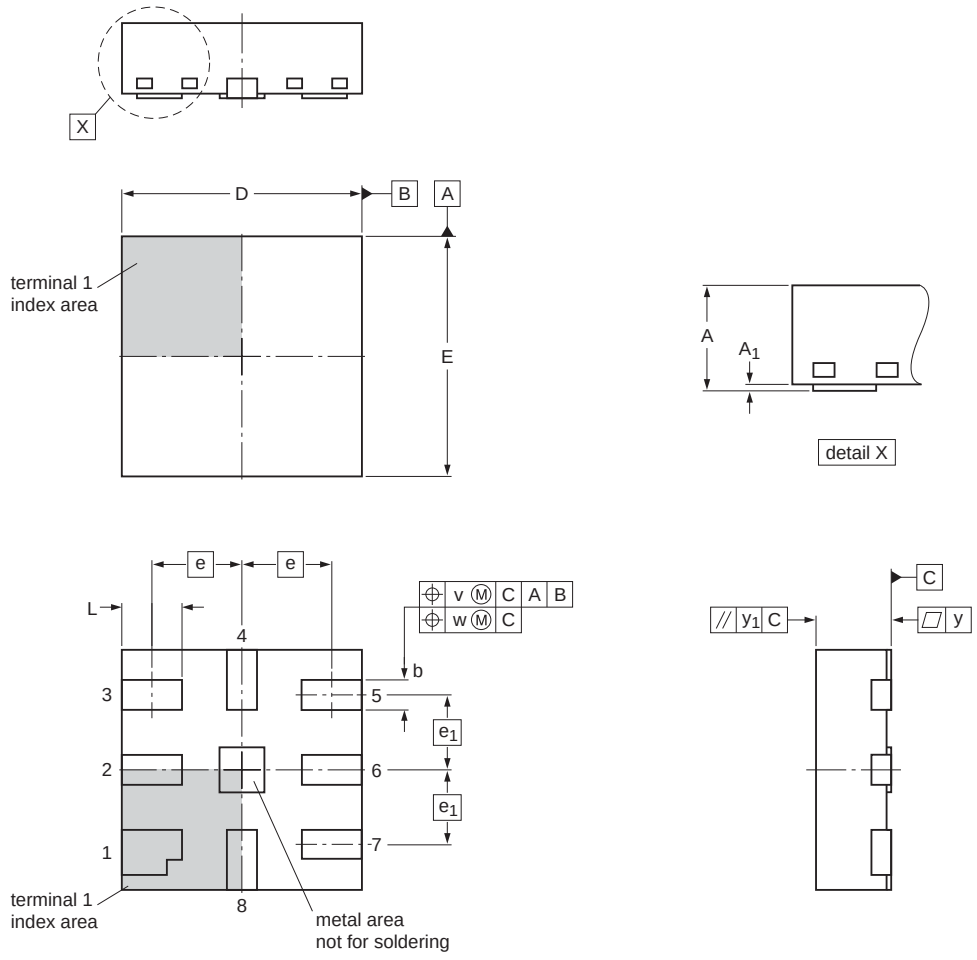
[2] Maximum VIH = VDD(max) + 0.5 V or 5.5 V, which ever is lower. See component data sheets.

[3] The same resistor value to drive 3 mA at 3.0 V VDD provides the same RC time constant when using <2 V VDD with a smaller current draw.

[4] Only applies to Fast Mode and Fast Mode Plus.

14. Package outline

XQFN8: plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm **SOT902-3**



Dimensions

Unit		A	A_1	b	D	E	e	e_1	L	v	w	y	y_1
mm	max	0.5	0.05	0.25	1.65	1.65			0.45				
	nom			0.20	1.60	1.60	0.6	0.5	0.40	0.1	0.05	0.05	0.05
	min		0.00	0.15	1.55	1.55			0.35				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot902-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT902-3	- - -	MO-255	- - -			~~11-08-16~~ 11-08-18

Fig 9. Package outline SOT902-3

15. Abbreviations

Table 18. Abbreviations

Acronym	Description
CRC	Cyclic Redundancy Check
CW	Continuous Wave
EEPROM	Electrically Erasable Programmable Read Only Memory
EPC	Electronic Product Code (containing Header, Domain Manager, Object Class and Serial Number)
FM0	Bhi phase space modulation
HBM	Human Body Model
IC	Integrated Circuit
LSB	Least Significant Byte/Bit
MSB	Most Significant Byte/Bit
NRZ	Non-Return to Zero coding
RF	Radio Frequency
RTF	Reader Talks First
Tari	Type A Reference Interval (ISO 18000-6)
UHF	Ultra High Frequency
X_{xb}	Value in binary notation
XX_{hex}	Value in hexadecimal notation

16. References

[1] I²C-bus specification and user manual (NXP standard UM10204.pdf / Rev. 03 - 19 June 2007)

[2] EPC Radio-Frequency Identity Protocols Class-1 Generation-2 UHF RFID Protocol for Communications at 860 MHz - 960 MHz Version 1.2.0

[3] EPC Conformance Standard Version 1.0.5

[4] ESD Method SNW -FQ-302A

[5] ISO/IEC 18000-1: Information technology - Radio frequency identification for item management - Part 1: Reference architecture and definition of parameters to be standardized

17. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SL3S4011_4021 v. 3.1	20130703	Product data sheet	-	SL3S4011_4021 v. 3.0
Modifications:	• General update			
SL3S4011_4021 v. 3.0	20130416	Product data sheet	-	SL3S4011_4021 v. 2.3
Modifications:	• Data sheet status changed to Product data sheet			
SL3S4011_4021 v. 2.3	20130305	Preliminary data sheet	-	SL3S4011_4021 v. 2.2
Modifications:	• General update • Security status changed into COMPANY PUBLIC			
SL3S4011_4021 v. 2.2	20121127	Preliminary data sheet		SL3S4011_4021 v. 2.1
Modifications:	• General update			
SL3S4011_4021 v. 2.1	20120726	Preliminary data sheet	-	SL3S4001FHK v. 2.0
Modifications:	• General update			
SL3S4011_4021 v. 2.0	20120627	Preliminary data sheet	-	SL3S4001FHK v. 1.2
Modifications:	• General update			
SL3S4001FHK v. 1.2	20111004	Objective data sheet	-	SL3S4001FHK v. 1.1
Modifications:	• Table 1 “Ordering information”: updated • Figure 3 “UCODE I2C wafer layout”: values updated			
SL3S4001FHK v. 1.1	20110707	Objective data sheet	-	SL3S4001FHK v. 1.0
Modifications:	• Table 3 “Mechanical properties XQFN8”: updated • Section 10.6 “Addressing”: updated			
SL3S4001FHK v. 1.0	20110609	Objective data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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